Patent Claims

1. A memory chip having a substrate (1), into which memory cells are introduced,
the memory cells having a trench capacitor (2) and a transistor,
the trench capacitor at least partially having a filling (3, 4), and
the transistor (22, 21, 28) having a source terminal and a drain terminal (21, 22) and a gate terminal (28),
the drain terminal (21) being electrically conductively connected to the trench capacitor (3, 4),
it being possible for the source terminal (22) to be conductively connected to the filling (3, 4) depending on a driving of the gate terminal (28),
characterized in that
the filling (3, 4) at least partially has a material which is unstable at high temperatures, in particular at temperatures of above 800°C.

2. The memory chip as claimed in claim 1, characterized in that the filling (3, 4) at least partially has a metallic material.

3. The memory chip as claimed in either of claims 1 and 2, characterized in that the filling (3, 4) at least partially has a dielectric material having a high dielectric constant.

4. The memory chip as claimed in one of claims 1 to 3, characterized
in that the wall of the trench (2) is at least partially covered with a dielectric layer (3),
in that a metallic layer (4) is at least partially applied

on the dielectric layer (3),
in that the metallic layer (4) is electrically conductively connected to the drain terminal (21) of the transistor via a strap filling (17).

5. The memory chip as claimed in one of claims 1 to 4, characterized in that an electrically conductive layer (5) is formed in a manner adjoining the trench (2) in the substrate (1).

6. The memory chip as claimed in one of claims 1 to 5, characterized
in that the trench is covered by an epitaxial layer (6),
in that an opening is introduced in the epitaxial layer (6),
in that a conductive connection between the filling (3, 4) and the drain terminal (21) is formed through the opening,
in that a dielectric layer (3) is at least partially applied on that side of the epitaxial layer (6) which faces the trench (2).

7. A method for fabricating a memory cell having a trench capacitor, having the following method steps of:
introducing a trench (2) into a substrate (1);
filling the trench (2) at least partially with a dummy filling (32);
applying a covering layer (6) to the substrate (1), which covering layer is preferably formed as an epitaxial layer;
introducing a transistor (21, 22) into the covering layer (6);
removing the dummy filling (32) from the trench (2);
introducing a storage dielectric (3) and a trench electrode (4) into the trench (2), a trench capacitor being created, and

forming a connection of the trench electrode (4) to a terminal (21) of the transistor.

8. The method as claimed in claim 7, characterized in that a channel (24, 57) is etched into the covering layer (6) as far as the dummy filling (32), in that the dummy filling (32) is etched out via the channel (24, 47, 57), in that a dielectric layer (3) is at least partially applied to the wall of the trench (2), in that a conductive layer (4) is applied to the dielectric layer (3), in that the conductive layer (4) is electrically conductively connected to a terminal (21) of the transistor.

9. The method as claimed in either of claims 7 and 8, characterized in that, after the etching of the channel (47, 57), the sidewalls of the channel (47, 57) are covered with a protective layer (62, 71), preferably made of nitride, in that the dummy filling (32) is subsequently etched out from the trench (2, 3).